Enhancement of In_2O_3 Field-Effect Mobility Up To 152 $cm^2 \cdot V^{-1} \cdot s^{-1}$ Using HZO-Based Higher-k Linear Dielectric

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Abstract

In this work, we report high-performance atomic-layer-deposited (ALD) In_2O_3 thin-film transistor (TFT) using $Hf_xZr_{1-x}O_2$ (HZO) as a linear higher-k dielectric. By properly inserting a thin Al_2O_3 layer between two HZO layers with asymmetric thickness and post-deposition annealing (PDA) of the HZO-Al_2O_3-HZO (HZAHZO) stack capped with In_2O_3, the k value of the linear dielectric is boosted to 30. This results in an equivalent oxide thickness (EOT) of 1.9 nm with physical thickness of 15.5 nm and meanwhile In_2O_3 field-effect mobility (μ_{FE}) is boosted to 152 $cm^2 \cdot V^{-1} \cdot s^{-1}$, simultaneously. Such enhancements enable high-performance TFTs with record saturation current (I_{sat}) exceeding 2 mA/μm with a channel length (L_{ch}) of 1 μm, and maximum current (I_{max}) reaches 7 mA/μm with L_{ch} of 30 nm. Higher-k dielectrics also enhance the electrostatic control of the channel with negligible hysteresis, on/off ratio over 10^{11}, and drain-induced barrier lowering (DIBL) less than 40 mV/V at L_{ch} of 35 nm. This work demonstrates a promising and straightforward methodology to enhance the mobility of oxide semiconductor (OS) channel by using linear higher-k dielectrics.

Introduction

From early 2000, extensive research on HfO_2-based high-k dielectrics (hafnia) paved the way for commercial adoption of hafnia in modern VLSI industry. The slowing of transistor's physical dimension scaling motivates the researchers to revisit on hafnia with a higher k value. The most stabilized phase of as-deposited HfO_2 by ALD is monoclinic (m) phase, which has a lower k value of around 14-20. But it can be greatly enhanced to above 45 in tetragonal (t) phase with a higher symmetry and effective charge, as shown in Fig. 1 [1-3]. To lower the t-phase transition temperature and enhance its stabilization, careful strain engineering and doping using around 10% Si/Ge/Al with small ionic radius or >50% Zr ratio are required, as depicted in Fig. 2 [3-6]. But these approaches still require a high-temperature process and unavoidably form a low-k inter-layer with Si, resulting in an increase of EOT and mobility degradation due to remote phonon scattering (RPS) [7, 8]. It is also not back-end-of-line (BEOL) compatible in terms of processing temperature.

ALD In_2O_3, featuring high drain current [9], low contact resistance [10], 3-D conformality [11] and stability under high-temperature process [12], is attracting growing interest for BEOL 3D integration. The main challenge of ultrathin OS is its amorphous nature with relatively low mobility. Currently, limited reports on OS TFTs with high mobility exceeding 100 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [13-19]. Enhancement of OS mobility is highly demanded.

In this work, we report a novel HZO-Al_2O_3-HZO linear dielectric with ALD In_2O_3 capping to achieve a higher k value of 30, low EOT below 2 nm with a physical thickness of 15.5 nm and enhance μ_{FE} of In_2O_3 over 150 $cm^2 \cdot V^{-1} \cdot s^{-1}$. This is ascribed to the dominant formation of t-phase in HZAHZO stacks and the significant reduction of remote Coulomb scattering (RCS) to the channel. Such enhancements enable high-performance OS-TFTs with negligible hysteresis, on/off ratio over 10^{11}, small sub-threshold swing (SS) and DIBL. The I_{sat} of TFTs exceeds 2 mA/μm with L_{ch}=1 μm, and I_{max} reaches 7 mA/μm with L_{ch}=30 nm.

Experiments

Figs. 3 and 4 show the device schematic diagram and fabrication process flow of higher-k HZAHZO-In_2O_3 TFTs based on ALD. A thin Al_2O_3 layer was inserted to break HZO into two asymmetric parts. Two HZAHZO stack orders (I and II), as demonstrated in Fig. 3, are investigated. The W/HZAHZO/In_2O_3 stack underwent a 350°C PDA under O_2 environment, which is critical to form polycrystalline t-phase in HZO and simultaneously passivate the oxygen vacancies in In_2O_3. Fig. 5(a) shows the high-resolution TEM (HRTEM) cross section view with EDS mapping of a short-channel TFT with stack I and L_{ch} of 30 nm, capturing W, Al, Zr, Hf, Zr, In and Ni elements. Stack-I HZAHZO with polycrystallinity is highlighted in Fig. 5(b).

Results and Discussion

Figs. 6(a) and (b) show the transfer characteristics of long-channel (L_{ch} of 2 μm) ALD HZAHZO-In_2O_3 TFTs with stack-I and II, respectively. Both log and linear-scale curves at linear region with V_{DS} of 0.1 V and saturation region with V_{DS} of 1 V are shown. Both stack I and II present negligible hysteresis. Compared with stack-II, stack-I HZAHZO TFTs have a more positive threshold voltage (V_{TH}), smaller SS and higher transconductance (g_m). The performance enhancement is mainly due to the higher k value of dielectric and the higher mobility of In_2O_3 channel in stack I. Fig. 7 demonstrates the C_g-V response of the two W/HZAHZO/In_2O_3 stacks at frequency of 100 kHz. With the same physical thickness, stack I achieves an EOT of 1.92 nm with k value of 30.2, higher than that of 21 in stack II. Minor hysteresis loops in stack I from large area capacitors indicates minor ferroelectric phase co-exhibiting in a large area. But the t- and m-phase dominate in stack I and II, respectively. Fig. 8 presents the μ_{FE} of the two stacks extracted from the g_m of Fig. 6 and C_g of Fig. 7. Compared with stack II, the stack-I HZAHZO enables a 34% increase in μ_{FE} from 113 $cm^2 \cdot V^{-1} \cdot s^{-1}$ to 152 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which is the record high mobility value ever reported in all OS TFTs. This mobility enhancement originates from the reduction of RCS potential due to the higher dielectric constant in stack I. Fig. 9 shows the simulation trend of reducing RCS rate with increasing k value. Fig. 10 shows the temperature-dependent transfer characteristics of a stack-I TFT with L_{ch} of 2 μm from 295 K to 10 K. The SS, g_m and I_{ON} of device presents a weak dependence on temperature. A negative threshold voltage (V_{TH}) shift and a reduction of C_g are observed in the inset of Fig. 11. The temperature dependence of μ_{FE} is calculated and presented in Fig. 11. The extracted μ_{FE} increases slightly to 175 $cm^2 \cdot V^{-1} \cdot s^{-1}$ under 100 K and remains constant until 10 K. This implies electron-phonon scattering is dominant in transport with high-quality In_2O_3.

The higher-k dielectrics with higher μ_{FE} also enhance the performance of short-channel devices. Fig. 12 shows the transfer characteristics of a stack-I TFT with L_{ch} of 35 nm with V_{DS} of 0.1 and 0.5 V. The transistor has an on/off ratio of 10^{11}, the negligible hysteresis, a low DIBL of 40 mV/V, and a small SS of 75 mV/dec. The I_{max} at V_{DS} of 0.5 V exceeds 2.75 mA/μm, indicating a good electrostatic control with higher-k HZAHZO stack. Figs. 13 and 14 show the output characteristics of stack-I TFT with L_{ch} of 1 μm and 30 nm, respectively, utilizing ultra-fast pulse I-V (UFPIV) measurement to alleviate self-heating effect [9]. For the device with L_{ch} of 30 nm, the cooling stage at 33 K is utilized to further dissipate heat. The stack-I HZAHZO-In_2O_3 TFTs presents a good saturation behavior in long-channel devices with I_{sat} exceeds 2 mA/μm at L_{ch} of 1 μm, which is the record high I_{sat} reported in long channel OS-TFTs. I_{max} reaches 7 mA/μm at V_{DS} of 1.2 V and V_{GS} of 3 V with L_{ch} of 30 nm. Figs. 15(a)-(d) show the scaling metrics of V_{TH}, SS, g_m, and I_{max}, with L_{ch} ranging from 2 μm to 30 nm, respectively, for both stack-I and II HZAHZO-In_2O_3 TFTs. The higher-k stack I stands out from stack II with a higher immunity to V_{TH} roll-off and SS degradation when L_{ch} scales. Stack-I HZHAZO also presents higher g_m and I_{max}.

Fig. 16 benchmarks the μ_{FE}, k value of dielectrics and I_{max} of currently reported OS-TFTs with mobility>90 $cm^2 \cdot V^{-1} \cdot s^{-1}$. This work highlights not only the record high μ_{FE}, but also the k value of gate dielectric, which leads to the highest current level among all these high-mobility OS-TFTs.

Conclusion

In conclusion, high-mobility OS-TFTs based on higher-k hafnia are demonstrated. The work has two discoveries: (1) properly incorporating a thin Al_2O_3 layer to divide HZO into two asymmetric parts and performing PDA with In_2O_3 capping. HZO becomes a linear dielectric with the k value of 30. (2) In_2O_3 channel mobility increases to over 150 $cm^2 \cdot V^{-1} \cdot s^{-1}$ because of the reduction of RCS with a higher-k dielectric. These enhancements lead to a record high I_{sat} exceeding 2 mA/μm with L_{ch} of 1 μm at room temperature and I_{max} reaches 7 mA/μm with L_{ch} of 30 nm at 33K. This work opens a new route to further improve the device performance of OS TFTs in general. The work is mainly supported by Samsung Electronics and AFOSR.

Reference: [1] X. Zhao et al., *Phys. Rev. B*, vol. 65, 075105, 2002. [2] X. Zhao et al., *Phys. Rev. B*, vol. 65, 233106, 2002. [3] C-K. Lee et al., *Phys. Rev. B*, vol. 78, 012102, 2008. [4] P. K. Park et al., *Appl. Phys. Lett.*, vol. 89, 192905, 2006. [5] J. Zhou et al., *IEDM*, 13.4, 2021. [6] Y-R. Chen et al., *EDL*, vol. 43, p. 1601, 2022. [7] M. Fischetti et al., *J. Appl. Phys.* 90, p. 4587, 2001. [8] W. Zhu et al., *TED*, vol. 51, p. 98, 2004. [9] Z. Lin et al., *ACS Nano*, 16, p. 21536, 2022. [10] C. Niu et al., *IEDM*, 37.2, 2023. [11] M. Si et al., *VLSIT*, TF2-4, 2021. [12] Z. Zhang et al., *VLSIT*, TF11-3, 2023. [13] B. K. Kim et al., *EDL*, vol. 42, p. 347, 2021. [14] Y. Magari et al., *Nat. Commun*.13, 1078, 2022. [15] C. K. Nguyen et al., *Adv. Mater. Interfaces* 10, 2202036, 2023. [16] S. Hooda et al., *VLSIT*, T17-1, 2023. [17] H. Y. Lee et al., *ACS Appl. Mater. Interfaces*, 15, 51399, 2023. [18] Y-S. Kim et al., *Small Methods 7*, 2300549, 2023. [19] K. Han et al., *EDL*, vol. 44, p. 1999, 2023.

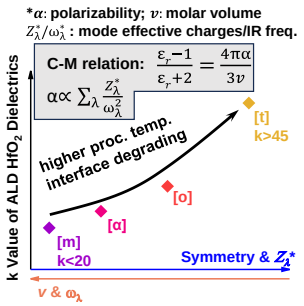

Fig. 1. k value evolution with different hafnia phases. Higher-k phases generally come with higher processing temperatures.

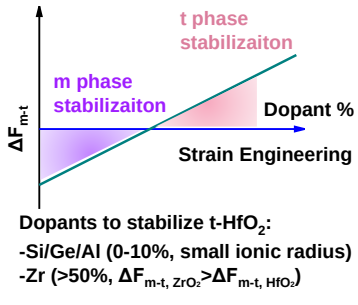

Fig. 2. Proper doping and strain engineering are required to stabilize t-phase hafnia at low temperature.

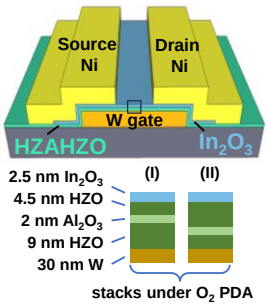

Fig. 3. Device schematics of HZAHZO-In_2O_3 TFTs, highlighting the two stacks under PDA.

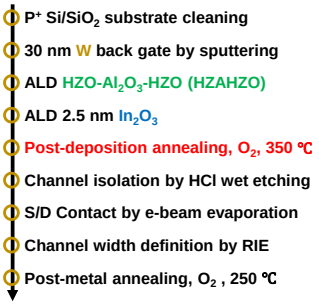

Fig. 4. Fabrication process flow of the higher-k HZAHZO-In_2O_3 TFTs.

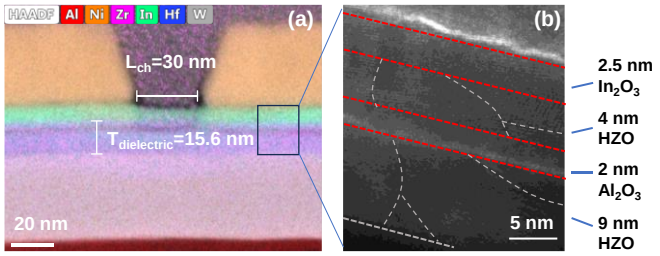

Fig. 5 (a) HRTEM cross-section image with EDS mapping of a higher-k HZAHZO-In_2O_3 TFT with L_{ch} of 30 nm. (b) The TEM image of stack I, highlighting the polystability and layered structure.

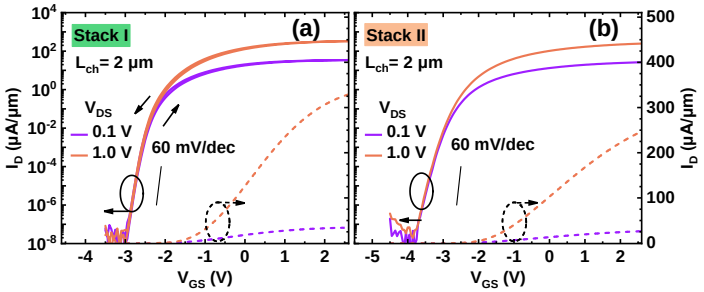

Fig. 6. Bi-directional transfer characteristics of 2-μm HZAHZO-In_2O_3 TFTs with stack-I (a) and II (b), at linear region with V_{DS} of 0.1 V and saturation region with V_{DS} of 1 V with negligible hysteresis.

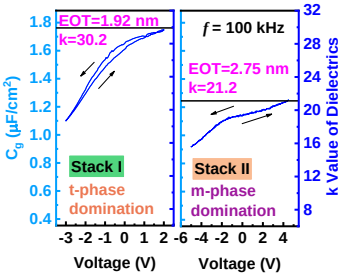

Fig. 7. C_g-V response of the W/ HZAHZO/In_2O_3 stacks I and II at a frequency of 100 kHz. The size of capacitor is large (8 μm x 8 μm) having minor ferroelectric o-phase.

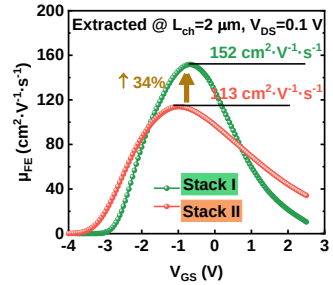

Fig. 8. Extracted μ_{FE} of the stacks I and II at L_{ch} of 2 μm, calculated from g_m of Fig. 6 and C_g of Fig. 7.

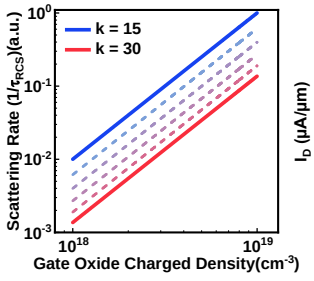

Fig. 9. Simulation of RCS scattering rate dependency on k value and gate oxide charge density.

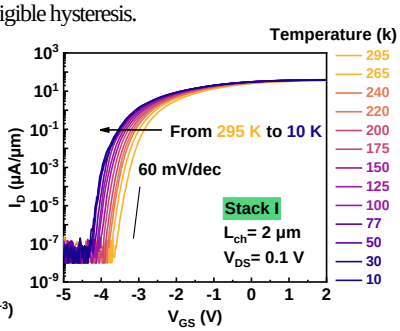

Fig. 10. Temperature-dependent transfer characteristics of stack-I TFTs with V_{DS} of 0.1 V and L_{ch} of 2

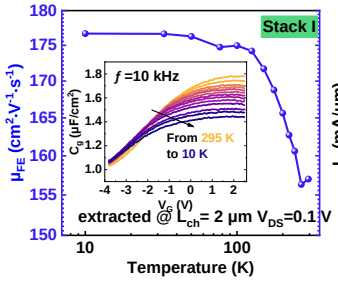

Fig. 11. Temperature dependence of extracted μ_{FE}. Inset: temperature-dependent C_g-V response of stack I.

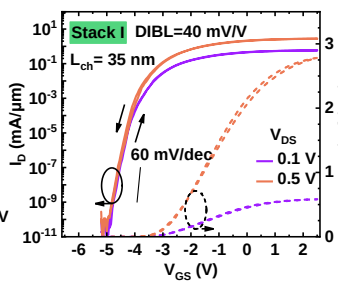

Fig. 12. Transfer characteristics of a stack-I TFTs with L_{ch} of 35 nm, at V_{DS} of 0.1 V and 0.5 V.

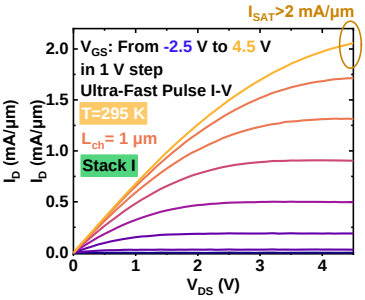

Fig. 13. UFPIV output characteristics of a stack-I TFTs with L_{ch} of 1 μm, highlighting I_{sat}>2 mA/μm.

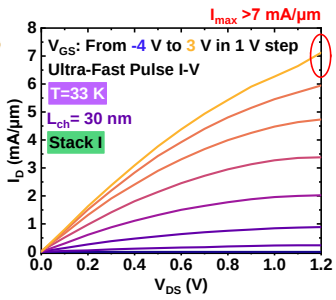

Fig. 14. UFPIV output characteristics of a stack-I TFTs with L_{ch} of 30 nm at 33K, highlighting I_{max}>7 mA/μm.

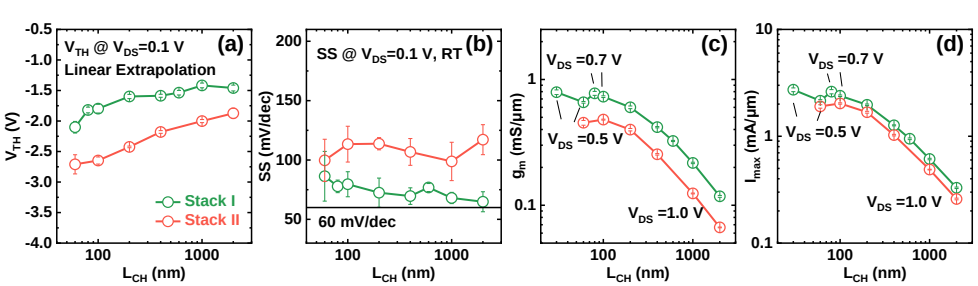

Fig. 15. Scaling metrics of (a) V_{TH}, (b) SS, (c) g_m, and (d) I_{max} for both stack-I and II HZAHZO-In_2O_3 TFTs. Each data points contains the characteristics of at least 5 devices fabricated on the same wafer.

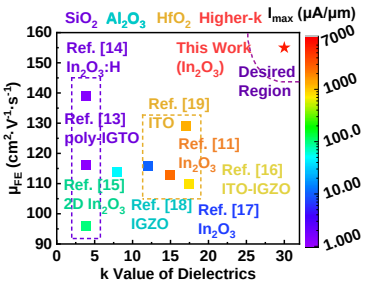

Fig. 16. Benchmarks of the μ_{FE}, k value of dielectrics and I_{max} of reported OS-TFTs